## PCI DEVICE RESOURCE ASSIGNMENT

<table>
<thead>
<tr>
<th>BUS</th>
<th>DEVICE</th>
<th>IDSEL</th>
<th>PCI_REQ#</th>
<th>PCI_GNT#</th>
<th>INT_IRQ#</th>
</tr>
</thead>
<tbody>
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<td>1</td>
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<td>5</td>
<td>REQ#4</td>
<td>GNT#4</td>
<td>IRQD#</td>
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<tr>
<td>1</td>
<td>CardBus</td>
<td>9</td>
<td>REQ#1</td>
<td>GNT#1</td>
<td>IRQB#</td>
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<tr>
<td>1</td>
<td>VIA1394</td>
<td>3</td>
<td>REQ#0</td>
<td>GNT#0</td>
<td>IRQF#</td>
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<tr>
<td>1</td>
<td>MiniPCI</td>
<td>6</td>
<td>REQ#2</td>
<td>GNT#2</td>
<td>IRQC# / IRQE#</td>
</tr>
</tbody>
</table>

**Notes:**
- IDSEL, PCI_REQ#, PCI_GNT#, and INT_IRQ# represent the resource assignment for each device.
- BUS 1 is used for LAN, CardBus, VIA1394, and MiniPCI.
This two cap should connect to VSSADAC first then to GND.
**CRT I/F & CONNECTOR**

**DDC_CLK & DATA level shift**

5V @ ext. CRT side

**Hsync & Vsync level shift**

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

**Ferrite bead impedance:** 75ohm@100MHz

**Layout Note:**
- Must be a ground return path between this ground and the ground on the VGA connector.
- 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

**CRT I/F & CONNECTOR**

**DDC_CLK & DATA level shift**

7 DAT, RED
7 DAT, GREEN
7 DAT, BLUE
R11, R20, R36 75k
R3, R9, R12 75k
L5, L6, L2 DLM11B750S
33 2.7uH
C323, C325, C327, C329 SC3P50V3CN
10uF
C324, C326, C328 SC3P50V3CN
10uF
U55A PACDN009
20K
R5, R42K 2.2R
R11, R87 75R
R11, R87 75R
R11, R87 75R
R11, R87 75R
C333 SCD1U16V
6.3V
C323, C325, C327, C329 SC100P
5.0V
L1, L2, L3 DLM11B750S
22uH
C10 SCD01U50V3KX
5V
D1 CH751H-40
2N7002
Q2, Q25 2N7002
U54A TSAHCT125
10KR
R328, R326, R327 10KR
R3 10KR
U1 TSLCXX125
150KR
7 DAT, HSYNC
1 DAT, VSYNC
DAC_RED7
DAC_GREEN7
DAC_BLUE7
DAC_VSYNC7
DAC_HSYNC7
3D3V_S0
5V_S0
6V_CRT_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
3D3V_S0
TV Encoder

CH7011A

**Layout 40 mil**

ESD Protection Diode

**TV_EMI**

B2M SC

TV Encorder - Chrontel 7011A

A3

13 43

Thursday, January 16, 2003

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**CH7011 Address:**

0x75 - AS pull-up (int. pull-up)

0x76 - AS pull-down

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**Power up default:**

NTSC - GPIO0 pull-up (int. pull-up)

PAL - GPIO0 pull-down

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75 Ohm close to chip

6 MHz; Low-Pass filter close to CONN

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Wistron Corporation
21F, 38, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan Hsien 221, Taiwan, R.O.C.

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TV Encorder - Chrontel 7011A

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IDE1 & IDE2

IDE Circuitry

Chipset

SMBUS2.0

SMBUS in S5 for SMBus 2.0 compliance

Wistron Corporation

21F, B8, Sec. 1, Han Ta Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
G768D thermal sensor & Fan controller

*Layout* 15 mil

CHECK DELAY TIME

EMI REQUEST,
PLACE BETWEEN DIFFERENT POWER PLANE.

HW Thermal Throttling
HDD Connector

CD-ROM CONN

CHECK PIDE/SIDE DIAG# PIN
100ohm 8100Hz

RTL 8100BL
71.08100.A0G

Close to RTL8100L
Pin60, Pin61

Second source: 72.93C46.D01 (ATMEL)

main source: 72.93C46.E01

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
**LAN Connector**

CLOSE TO TRANSFORMER

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

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**W/S:**
10/100 @ Surface layers
10/20 @ Inner layers

**Green LED:** Speed 100: ON/Speed 10: OFF
**Yellow LED:** Link: ON
The object of using S3 power plane is to support WakeOnLAN function of POMICA LAN Card.
Analog 0~5V Signal Quick Switch

CD AUDIO PATH SWITCH

CD-Play Mode
Always Install

Non CD-Play Mode

NEAR AUDIO OP

NEAR CR-ROM

CD-ROM Audio Lines
CDR/L/AGND PreAMP

NEAR CD ROM

Audio AMP and Jack
Unused FGPI pins must not be float.
Place CAPs close to CONN
Place near Printer Port for ext. FDD need
if $V_{th} = 100\, \text{mV}$, $V_{ilm}/10 = V_{th} = 100\, \text{mV}$

$V_{ilm} = 1\, \text{V} = 5\, \mu\text{A} \times R$, $R = 200\, \text{k}\Omega$

$2.5\, \text{V}$ ($I = 3.7\, \text{A}$, $OCP: 5.8\, \text{A}$)

$V_{adj} = 1.28\, \text{V}$

$V_{refout} = 1.25\, \text{V}$

DDR $V_{REF}$ must be near NB and DIMM

$2.5\, \text{V}$ ($I = 3.7\, \text{A}$, $OCP: 5.8\, \text{A}$)

$V_{adj} = 1.28\, \text{V}$

DDR $V_{REF}$ S3 need 10 mil and must be near NB and DIMM

$V_{adj} = 1.28\, \text{V}$
SYSTEM DC/DC
3D3V_S5/5V_S5/1D5V_S5

I_{\text{max}} = 300 \text{ mA}
I_{\text{max}} = 120 \text{ mA}

Double Layout
Imax = 2.0V/(20*0.02 ohm) = 5A

60W
R1469=100K, R1468=140K, R1465=0
Imax=2.98A
AD POWER=19*2.98=56.62W

70W
R1469=100K, R1468=140K, R1465=75K
Imax=3.49A
AD POWER=19*3.49=66.31W

notice sense resistor noise and trace

*Layout* 15 mil

*Layout* 15 mil
MicroChip Part Number
PIC16F872 : 71.46872.00I
PIC16F73 : 71.16F73.00I

Add "CDPLAY_SW" & "CD5V_OFF#/ON" for NARI

Adaptor IN Detection
CPU VID(1D2V)

SPEC. FOR DT NORTHWOOD CPU =>150mA
FOR MB NORTHWOOD CPU =>300mA

Run Power

Suspend Power

Support standby wakeup LAN only
Adaptor in to generate DCB\text{ATOUT}

*Layout*

150mil

CHANGE 4435A

BATTERY CONNECTOR

SB_EMI

SB_EMI