<table>
<thead>
<tr>
<th>DEVICE</th>
<th>IDSEL</th>
<th>IRQ</th>
<th>REQ# / GNT#</th>
</tr>
</thead>
<tbody>
<tr>
<td>TI 1394</td>
<td>AD19</td>
<td>Auto</td>
<td>REQ2# / GNT2#</td>
</tr>
<tr>
<td>MINIPCI SLOT</td>
<td>AD21</td>
<td>C, E</td>
<td>REQ3# / GNT3#</td>
</tr>
<tr>
<td>PCMCIA TI 1410</td>
<td>AD25</td>
<td>B, D</td>
<td>REQ1# / GNT1#</td>
</tr>
<tr>
<td>AGP</td>
<td>AD17(Int.)</td>
<td>A, B</td>
<td></td>
</tr>
<tr>
<td>LAN</td>
<td>AD24(Int.)</td>
<td>E</td>
<td></td>
</tr>
<tr>
<td>USB</td>
<td>AD29</td>
<td>A, D, C</td>
<td></td>
</tr>
<tr>
<td>Hub-to-PCI</td>
<td>AD30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPC Bridge/ IDE/AC9 7/ IDEbus</td>
<td>AD15</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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SERIES DAMPING
PLACE RHs CLOSE TO DM1 < 0.75";
STRGT DUAL LENGTH LIMITATION WITH DDS, CB PINS

M_DATA4 4
M_DATA4 3
M_DATA4 2
M_DATA4 1
M_DATA4 0
M_DATA3 8
M_DATA3 7
M_DATA_R 37
M_DATA_R 36
M_DATA_R 35
M_DATA_R 34
M_DATA_R 33
M_DATA_R 32
M_DATA_R 31
M_DATA_R 30
M_DATA_R 29
M_DATA_R 28
M_DATA_R 27
M_DATA_R 26
M_DATA_R 25
M_DATA_R 24
M_DATA_R 23
M_DATA_R 22
M_DATA_R 21
M_DATA_R 20
M_DATA_R 19
M_DATA_R 18
M_DATA_R 17
M_DATA_R 16
M_DATA_R 15
M_DATA_R 14
M_DATA_R 13
M_DATA_R 12
M_DATA_R 11
M_DATA_R 10
M_DATA_R 9
M_DATA_R 8
M_DATA_R 7
M_DATA_R 6
M_DATA_R 5
M_DATA_R 4
M_DATA_R 3
M_DATA_R 2
M_DATA_R 1
M_DATA_R 0
M_DATA 6
M_DATA 5
M_DATA 4
M_DATA 3
M_DATA 2
M_DATA 1
M_DQS 8
M_DQS 7
M_DQS 6
M_DQS 5
M_DQS 4
M_DQS 3
M_DQS 2
M_DQS 1
M_DQS 0
M_WE#8
M_WE#7
M_WE#6
M_WE#5
M_WE#4
M_WE#3
M_WE#2
M_WE#1
M_WE#0
M_CB_R 7
M_CB_R 6
M_CB_R 5
M_CB_R 4
M_CB_R 3
M_CB_R 2
M_CB_R 1
M_CB_R 0
M_CB 7
M_CB 6
M_CB 5
M_CB 4
M_CB 3
M_CB 2
M_CB 1
M_CB 0
M_A2
M_A1
M_A0
M_CS2_R# 7,10
M_CS2_R# 6,9
M_CS2_R# 5,8
M_CS2_R# 4,7
M_CS2_R# 3,6
M_CS2_R# 2,5
M_CS2_R# 1,4
M_CS2_R# 0,3
M_A_SR_12
M_A_SR_11
M_A_SR_10
M_A_SR_9
M_A_SR_8
M_A_SR_7
M_A_SR_6
M_A_SR_5
M_A_SR_4
M_A_SR_3
M_A_SR_2
M_A_SR_1
M_A_SR_0
M_CAS_SR# 12
M_CAS_SR# 11
M_CAS_SR# 10
M_CAS_SR# 9
M_CAS_SR# 8
M_CAS_SR# 7
M_CAS_SR# 6
M_CAS_SR# 5
M_CAS_SR# 4
M_CAS_SR# 3
M_CAS_SR# 2
M_CAS_SR# 1
M_CAS_SR# 0
M_RAS_SR# 12
M_RAS_SR# 11
M_RAS_SR# 10
M_RAS_SR# 9
M_RAS_SR# 8
M_RAS_SR# 7
M_RAS_SR# 6
M_RAS_SR# 5
M_RAS_SR# 4
M_RAS_SR# 3
M_RAS_SR# 2
M_RAS_SR# 1
M_RAS_SR# 0

PARALLEL TERMINATION
PULL NH STUBS < 0.8", PLACE RHs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

M_DATA1 4
M_DATA1 3
M_DATA1 2
M_DATA1 1
M_DATA1 0
M_DATA 6
M_DATA 5
M_DATA 4
M_DATA 3
M_DATA 2
M_DATA 1
M_DQS 8
M_DQS 7
M_DQS 6
M_DQS 5
M_DQS 4
M_DQS 3
M_DQS 2
M_DQS 1
M_DQS 0
M_WE#8
M_WE#7
M_WE#6
M_WE#5
M_WE#4
M_WE#3
M_WE#2
M_WE#1
M_WE#0
M_CB_R 7
M_CB_R 6
M_CB_R 5
M_CB_R 4
M_CB_R 3
M_CB_R 2
M_CB_R 1
M_CB_R 0
M_CB 7
M_CB 6
M_CB 5
M_CB 4
M_CB 3
M_CB 2
M_CB 1
M_CB 0
M_A2
M_A1
M_A0
M_CS2_R# 7,10
M_CS2_R# 6,9
M_CS2_R# 5,8
M_CS2_R# 4,7
M_CS2_R# 3,6
M_CS2_R# 2,5
M_CS2_R# 1,4
M_CS2_R# 0,3
M_A_SR_12
M_A_SR_11
M_A_SR_10
M_A_SR_9
M_A_SR_8
M_A_SR_7
M_A_SR_6
M_A_SR_5
M_A_SR_4
M_A_SR_3
M_A_SR_2
M_A_SR_1
M_A_SR_0
M_CAS_SR# 12
M_CAS_SR# 11
M_CAS_SR# 10
M_CAS_SR# 9
M_CAS_SR# 8
M_CAS_SR# 7
M_CAS_SR# 6
M_CAS_SR# 5
M_CAS_SR# 4
M_CAS_SR# 3
M_CAS_SR# 2
M_CAS_SR# 1
M_CAS_SR# 0
M_RAS_SR# 12
M_RAS_SR# 11
M_RAS_SR# 10
M_RAS_SR# 9
M_RAS_SR# 8
M_RAS_SR# 7
M_RAS_SR# 6
M_RAS_SR# 5
M_RAS_SR# 4
M_RAS_SR# 3
M_RAS_SR# 2
M_RAS_SR# 1
M_RAS_SR# 0

PLACE BETWEEN DM1, DM2
CLOSE TO DM2 < 0.2", TO DM1 < 1.1"
EQUAL LIMITATION WITH SCK/SCS#
PLACE ONE CAP CLOSE TO EVERY 2 PULL-UP TERMINATION RESISTORS, CRB P13
DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD (13)=107
0.1UF 0603 Y5V 27X

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN
**CRT I/F & CONN**

**Ferrite bead impedance:** 75ohm@100MHz

**Layout Note:**
* Must be a ground return path between this ground and the ground on the VGA connector.
* 37.4% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

**DDC_CLK & DATA level shift**

5V @ ext. CRT side

**Hsync & Vsync level shift**

Signal level need check.

---

**DDC_CLK & DATA level shift**

- LV50, LV50, LV50
- RS71, 15Kd
- R44, 15Kd
- R3, 15Kd

**Hsync & Vsync level shift**

- SV_S3
- R293, 220Kd
- R2, 39Kd
- L2

**Geometry Change from 440453-1-U1 -> 440453-1-U2**

**Notes:**
- Must be a ground return path between this ground and the ground on the VGA connector.
- 37.4% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

---

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2F, 66, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taoyuan County, Taiwan, R.O.C.
This signal has a weak int. pull-down. If the signal is sampled low, the ICH3 will set the CPU speed strap p. line for safe mode.

System designers should include a pull-down resistor on EN_PCP# but do not populate the r. resistor.

IC8(M) # TOP-SWAP OVERI2 CE Rising Edge of PW) This signal has a weak int. pull-up. If the signal is sampled high, this indicates that the system is strapped to the "TOP-SWAP" mode (ICH3 will assert All f or all cycles targeting PW) B00(S) spacing). Note that SW will not be able to clear th e Top-up bit until the system is rebooted w/o SM8A(M) being pulled down.

The signal is sampled low (default to weak int. pull-down), the termination scheme will be set to source. If t his signal is sampled high (via a n ext. pull-up to Vcc), the termination scheme will be set to parallel.

No RBB OOT Rising Edge of PW) This signal has a weak int. pul l-down. If the signal is sampled high, this indicates that the system is strapped to the "No Boot" mode (ICH3 will disable the S 0 Timer system reboot (fast use).
**LAN 82562**

**SSOP48**

*Optional Cap: value 6pF - 12pF if needed for magnets*

**CREATE TERMINATION PLANE - 1500pF - reference to chassis GND**

LAN_CLK: 50MHz for 100 BASE-T
5MHz for 10 BASE-T

ADV10 has its own internal pull-down resistor. Crystal away from magnets.

A floating termination plane is cut out from power plane layer which acts as a plane of capacitance with an adjacent ground plane.

Chassis GND should cover part of magnetics.

For Modem Cable from MDC Pulse H0013

Bob Smith Termination

A floating termination plane is cut out from power plane layer which acts as a plane of capacitance with an adjacent ground plane.
PCMCIA Controller

TI 1410A

SE: Change Geometry
Same as C-2
Name as C-2
Remark: Add AC-Link Isolation signal
POWER GENERATE

*Layout*
20 mil

AD1881A AC97 A AUDIO CODEC

*Layout*
AUDIO(analog)
(10,10) mil

BEEP SOUND LOGIC

*Layout*
locate near audio
moat opening 6 mil

*Layout*
20 mil
Unused FGPI pins must not be float

Boot Device must have ID [3:0] = 0000
Has internal pull-down resistors
All may be left floated

FWH_INIT#
LPC_LFRAME#
EXT_FWH#
FWH_INIT#
EXT_FWH#
PCIRST2#
PCIRST2#
LPC_LFRAME#
PCLK_DEBUGBD
PCLK_DEBUGBD
FWH_TBL#
5V_S0
3.3V_S0
3.3V_S0
5V_S0
3.3V_S0
1.85V_S0
3.3V_S0
1.85V_S0
1.85V_S0
FWH_FGPI4
FWH_FGPI3
FWH_FGPI2
FWH_FGPI1
FWH_FGPI0
FWH_WP#
FWHRST#
SELECT_FWH
FWH_FGPI4
FWHRST#
SELECT_FWH
FWH_FGPI3
FWH_FGPI2
FWH_FGPI1
FWH_FGPI0
FWH_WP#
LPC_LAD[0..3] 18,30,31,42
PCLK_FWH3
BC138
DUMMY-C3
R188
DUMMY-R3
Q23
MMBT3 904-U
BC139
DUMMY-C3
R188
DUMMY-R3
Q23
MMBT3 904-U

if $V_{th} = 100 \text{mV}$, $V_{ilm} = V_{th} = 100 \text{mV}$

$V_{ilm} = 1 \text{V} = 5 \mu \text{A} \times R$, $R = 200 \text{k} \text{ohm}$

$2.5 \text{V}$ ($I = 3.7 \text{A}$, $O \text{ CP: } 5.8 \text{A}$)

ADD 3 VIAS FOR TC22 (PWR & GND)

Resistor Rating

500mA rating

ADD 3 VIAS FOR TC22 (PWR & GND)

CLOSE TO & PIN

CONTACT DIRECTLY ADD 3 VIAS FOR PIN

Resistor Rating

500mA rating

ADD 3 VIAS FOR TC22 (PWR & GND)

CLOSE TO & PIN

CONTACT DIRECTLY ADD 3 VIAS FOR PIN

Resistor Rating

500mA rating

ADD 3 VIAS FOR TC22 (PWR & GND)

CLOSE TO & PIN

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500mA rating

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CONTACT DIRECTLY ADD 3 VIAS FOR PIN

Resistor Rating

500mA rating

ADD 3 VIAS FOR TC22 (PWR & GND)

CLOSE TO & PIN

CONTACT DIRECTLY ADD 3 VIAS FOR PIN

Resistor Rating

500mA rating

ADD 3 VIAS FOR TC22 (PWR & GND)

CLOSE TO & PIN

CONTACT DIRECTLY ADD 3 VIAS FOR PIN

Resistor Rating

500mA rating
To make sure the delta-V between 3D3V_S5 & 1D8V_S5 power plane will not exceed 2V at any time.
I\text{charge(max)} = 2.8\text{A} 4\text{S2P/3S3P}

Adaptor in to generate D\text{CB\text{A}T\text{O}U\text{T}}

I\text{charge(max)} = 2.66\text{A} 3\text{S2P}

Should be fine tune for accurancy

For SB charging current 2.3\text{A}

Should change AD+,AD+2 connection

Ver: SD

Ver: SC
Change to IMN10
New Pat, Need PN

In 01218-2, R374 is DUMMY
Must be changed to 2SD1383K

R45 is 90.9K
PN: 64.90925.651

100 m ohm
Adaptor IN Detection

AC_CURRENT

Ver: SC

MicroChip Part Number
PIC16F872 : 71.46872.00I
PIC16F73 : 71.16F73.00I