Modify to U40#AF1 power to +1.05V_MPLL as CRB change
DDRII DUAL CHANNEL A, B.

DDRII A CHANNEL

DDRII B CHANNEL

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

Uninstall

+0.9VSMVTT

[11, 10] M_A_ODTO
[11, 10] M_A_GN
[11, 10] M_A_BS

[7, 10] M_B_BS#1
[7, 10] M_B_BS#0

[7, 10] M_A_CAS#0
[7, 10] M_A_RAS#0

+3V

DDR2 termination

R184
R186

C780*0.01U/16V

R541*200

C58

U5*LM86CIMM

MLF8_3V

CGCLK_SMB

CGDAT_SMB

SCLK

PM_EXTTS#0

PM_EXTTS#1

ALERT#6

OVERT#4

PM_EXTTS#1_D

DDR_THERMDA

DDR_THERMDC

Quanta Computer Inc.

PROJECT : QT6

Date: Sheet

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NVVDD Decoupling

Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence

PXE 1.2VDD
PXE 1.1VDD
I/O 3.3V
NV9X
1.8VFBDDQ
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

Keep pin 5 NC to prevent burning

SI-2
Change Pin define 12/18

Delete CN20, R63, C761(Remove Logo light2)
Audio Amplifier

Swap Audio input source as Speaker Bo noise issue
Change R468, R469 from 20K to 0 ohm as HP request

Audio Amplifier

Add in SI-2
- Add C918, U46, R528, R733, R740, C916, C653, C650
  for PC-Sweep function
- R528, C916 change to no-stuff for SI-2 test --&gt;12/6

Gain Table

<table>
<thead>
<tr>
<th>GAIN0</th>
<th>GAIN1</th>
<th>AV</th>
<th>RIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>60B</td>
<td>90K</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>15.6dB</td>
<td>45K</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>21.6dB</td>
<td>25K</td>
</tr>
</tbody>
</table>

Mute LED

Change Power source to +5VPCU as power situation

Accelerometer Sensor

Change R181 to no stuff as internal pull high
LED PWR CONTROL

Change Q12 to AO3404 as LED current limited

PV Build
Add R817, R818, R819 as HP LED spec change
Add C964 for reserve
**BLUETOOTH**

**PV Build**
Change CN14 P/N to DFHD06MR590

- **CN14 BLUE TOOTH CONN**
  - Change footprint as MB request (pitch 1.25mm to 1.0mm)

**Touch Screen**

Delete Touch-Screen in SI-2
CNO, C10, L4

**USB CAMERA /DIGITAL MIC CONNECT**

**SI-2 Build**

- **CN9**
  - Change Footprint to 88266-0600-6P-L-QT6
- SI-2 CAMERA BOARD
  - Fixed input Voltage 0823

**SI-2**

Add for EMI solution

**USB fingerprint CON**

**PV Build**

- Change Pin define 0823
  - DFVF05MS0506

- **DFHD06MR590**
  - Vout=1.25 (1+R1/R2)

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

**LEFT SIDE USBX1 and E-SATA/USB COMBO**

**RIGHT SIDE USBX2**
For 8102E/8111C

- New add and close to Pin 5
  From Vendor EMI suggest
- SI-2 R43
  No Mount, R247 mount
- U18863 wider than 40 mils
- U18881 wider than 60 mils

PV Build
Remove 811B and 8101E support in PV Build
1. Delete R264 (For 811B)
2. Delete R655 and T2Z
3. Delete R651 and U18#33 for 811B support
4. Delete R221 as RSET
5. Delete R242, R243, R244, R245, C394, C395 8101E support

for 93C56 used, NC if 93C46 is used.
For 8102E

For Giga must change L65 to Inductor (Chipset include switch power)
CTRL18 will become to switch power phase

For 8102E

8111C CV-4708MN00
8102E CS000044A0

For 8111C(P)
RTL8111C(P)
RTL8102E
LANVCC 3.3V
LAN_D1.8 1.2V
LAN_A1.8 1.2V
LAN_D1.5 1.2V

LAN Power domain chart

LAN-VCC pins-16, 37, 46 and 53. placement close lan chip
LAN_D1.5 pins- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58. placement close lan chip
LAN_A1.8 pins-5, 8, 11 and 14. placement close chip

only for 8111C application

For 8102E

Remove R250, L63, L66 --> For 8102E

SI-2

L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%

L65 4.7uH_2016

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Change CN15#31,32 to O3 as hole request for hole pad

Modify Pin Gnd as SMT request

SI-2 add Pin 21-25 as U25 Thermal pad tied to Gnd

For HP request to reserve

PROJECT : QT6
Quanta Computer Inc.
Delete R78 and tie the CN23624 to R110 direction.
Change CN23 layout footprint to MPCE-E-A50B223-S40N-7F-S2P-QT6 as ME drawing.
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
Countinue current: 5A
Peak current: 7.5A
OCP minimum 9A

3.3 Volt +/- 5%
Countinue current: 5A
Peak current: 7.5A
OCP minimum 10A
VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current: 7.5A
Peak current: 10A
OCP minimum 15A

RDSon=15m ohm

Vo=0.75 (R1+R2) / R2

Vo=0.75 (R1+R2) / R2

+1.05V/+1.5V (RT8204)

1AB

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1.8 Volt +/- 5%
Countinue current: 6A
Peak current: 14A
OCF minimum 17A

For Discrete Only
1.1 Volt +/- 5%
Countinue current: 2A
Peak current: 3A

PV Build
Change PR122 tied to 1.8V_ON as power sequence request