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</table>
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDL_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.

VLDT_RUN

VLDT_A2, VLDT_B2, VLDT_A1, VLDT_B1

L0_CTLOUT_H0, R2

HT_CTLIN0_P (9)

HT_CPU_CTLOUT1_P

C1

VLDT_RUN, HT_CTLOUT, HT_CPU_CTLOUT, R1

ATHLON64 HT I/F

QUANTA COMPUTER

LAYOUT: Place bypass cap on topside of board near HT power pins that are not connected directly to downstream HT device, but connected internally to other HT power pins. Place close to VLDT0 power pins.

ATHLON 64 S1 Processor Socket
POWER
Athlon 64 S1
Processor Socket

GROUND
Athlon 64 S1
Processor Socket

BOTTOMSIDE DECOUPLING

+1.8V_SUS

DECcoupling BETWEEN processor AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.8V_SUS

add more two 180pCap as AMD suggestion

PROCESSOR POWER AND GROUND
RTT termination changed from 56 ohm to 47 ohm as AMD suggestion.
SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

1.2 PLAN FSB UNDER THIS PLAN

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN
SB600 has 15K internal PU for AC_SDOUT
15K internal PU for RTC_CLK
External PU/PD is not required.

**REQUIRED STRAPS**

<table>
<thead>
<tr>
<th>PULL</th>
<th>AC_SDOUT</th>
<th>RTC_CLK</th>
<th>PCI_CLK4</th>
<th>PCI_CLK6</th>
<th>PCI_CLK0</th>
<th>PCI_CLK1</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH</td>
<td>USE DEBUG STRAPS</td>
<td>INTERNAL RTC</td>
<td>USE INT. PLL48</td>
<td>CPU IF=P4</td>
<td>H, H = PCI ROM</td>
<td>L, L = LPC ROM</td>
</tr>
<tr>
<td>LOW</td>
<td>IGNORE DEBUG STRAPS</td>
<td>EXTERNAL RTC</td>
<td>USE EXT. 48MHZ</td>
<td>CPU IF=I4</td>
<td>DEFAULT</td>
<td>DEFAULT</td>
</tr>
</tbody>
</table>

**DEBUG STRAPS**

<table>
<thead>
<tr>
<th>PDACK</th>
<th>PCI_AD28</th>
<th>PCI_AD27</th>
<th>PCI_AD26</th>
<th>PCI_AD25</th>
<th>PCI_AD24</th>
<th>PCI_AD23</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH</td>
<td>USE LONG RESET</td>
<td>DEFAULT</td>
<td>USE PCI PLL</td>
<td>USE ACPI BCLK</td>
<td>USE IDE PLL</td>
<td>USE DEFAULT PCIE STRAPS</td>
</tr>
<tr>
<td>LOW</td>
<td>USE SHORT RESET</td>
<td>DEFAULT</td>
<td>BYPASS PCI PLL</td>
<td>BYPASS ACPI BCLK</td>
<td>BYPASS IDE PLL</td>
<td>USE EEPROM PCIE STRAPS</td>
</tr>
</tbody>
</table>

SB600 has 15K INTERNAL PU FOR PCI_AD[28:23]
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

VSYNC(11)  
VGA_BLU(11)  
VGA_RED(11)  
VGA_GRN(11)

Page 6 has some change for DDCCLK & DDCDAT.

C377*22P_NC  
C378*10P_NC  
C379*10P_NC  
C380*10P_NC  
C381*10P_NC  
C382*10P_NC  
C383 10P/50V/0402  
C384 10P/50V/0402  
C385*10P_NC  
C386*10P_NC  
C387*22P_NC  
C388*22P_NC  
C374 .01U/25V/0402  
C375*22P_NC  
C376*22P_NC  
C377*22P_NC  
C378*10P_NC  
C379*10P_NC  
C380*10P_NC  
C381*10P_NC  
C382*10P_NC

L34BLM21PG220SN1D  
L35BLM21PG220SN1D  
L36BLM21PG220SN1D  
L37BLM11A121S  
L38BLM11A121S

R354 150/F_0402  
R355 150/F_0402  
R356 150/F_0402  
R357 39_0402  
R358 0_0402  
R359 1K_0402  
R360 39_0402

D11CH501H-40PT  
D11A91-ND200-7F  
D12  
D13CH501H-40PT  
D13CH501H-40PT  
D13  
D14  
D15

U1274AHCT1G125GW  
U1374AHCT1G125GW

T117PAD

delete Svideo for defeature
Route CBUS_GRST# to GPIO03 (pin 94) of the S10 companion chip EC8501L, and name the signal CBUS_GRST#.

If CBUS_GRST# is controlled by the system, then CBUS does not need to apply.

If R374 is populated, both C402 and R377 can be depop.

CBUS_GRST# should be asserted only when system power supply is on.

The ICH schematic need to include a pull-up resistor to implement CBUS#, and the ICH schematic must have a pull-down, or constantly drive the signal low, in order to fixable CBUS#.

Refer to DELL R07 schematic E06
deleted 1394 for defeature

80 mils

Place these caps as close to the U15 as possible.

5. TPBN1 & TPBP1, Short to GND if the 1394 Port Is Not Used.

changed for SD/MMC/SDIO only

IEEE1394/SD

U15A

R5C832T_V00

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
TPBIAS0 113
TPBN0 104
TPBP0 105
TPAN0 108
TPAP0 109
XI94
XO95
FIL096
REXT101
VREF100

MDIO00 80
MDIO13 90
MDIO03 77
MDIO04 76
MDIO05 75
MDIO06 74
MDIO07 73
MDIO08 88
MDIO09 84
MDIO10 82
MDIO11 81
MDIO12 93
MDIO01 79
MDIO02 78
MDIO14 91
MDIO15 89
MDIO16 92
MDIO17 87
MDIO18 85
MDIO19 83
AVCC_PHY4 112
RSV97

C424 1U/10V/0402
C419 01U/25V/0402
C425 1000P/50V/0402
L43BLM18PG181SN1D
C423 10U/10V/0805
C425 1000P/50V/0402

3. AVCC_PHY1, connection with +3.3V_R5C832 power
4. AVCC_PHY1, Inductor Required between +3.3V_R5C832 and AVCC_PHY

+3.3V_RUN_PHY
SD_CD# (22)
SD/XD/MS_CLK (22)
SD/XD/MS_DATA3 (22)
SD/XD/MS_DATA2 (22)
SD/XD/MS_DATA1 (22)
SD/XD/MS_DATA0 (22)
SD/XD/MS_DATA3 (22)
SD/XD/MS_CMD (22)
SD_WP#(XDR/B#) (22)
MC_PWR_CTRL_0 (22)
3 IN 1 CARD READER

DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only

For SD/MS power

6.150k Ohm Register
Required between SD/MMC_VCC and GND
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will add the 3.3V supply from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:

SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

Note: reserve L66 for current measurement, can be removed and short directly after RTS; and change +5V_RUN to +5V_ODD for ODD side power.
PCI-Express TX and RX direct to connector

Added C458 per EMI requirement.

Delete pin 17 for media board defeature ; delete pin 19 & 42, the 8051 debug signal

PCI-Express IV for defeature

Waiting to check

- change name for ED5
- copy ED5 to FX2
- Waiting to check
Express Card

NEW CARD GUIDE POST

+3V_CARD

PCI-Express TX and RX direct to connector

TH3: H-CH1D16G0S-4
TH3: H-CH1D16G0S-4

+3V_CARD

NEW CARD_PCIE_WAKE

JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

change name for ED5
copy ED5 to FX2
Waiting to check

+3.3V_SUS
+3V_CARD
+3.3V_RUN
+3.3V_CARDAUX
+1.5V_CARD
+1.5V_RUN
+1.5V_CARD
+1.5V_CARD
+1.5V_CARD
+1.5V_CARD
+1.5V_CARD
+1.5V_CARD

0427 : change from only net name to symbol "power point"
MDC INTERFACE

MDC Layout Notes
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Keep out area from Tip and Ring to other signals = 100 mils
4. Route Tip and Ring on one layer only (top or bottom)
5. Module internal cables wire size = 26 AWG (stranded or twisted pair wire)

EMI SOLUTION

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Keep out area from Tip and Ring to other signals = 100 mils
4. Route Tip and Ring on one layer only (top or bottom)
5. Module internal cables wire size = 26 AWG (stranded or twisted pair wire)

Place R117 close to J5
Place C23, C24 close to CON1

EMI requirement on 0812

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Keep out area from Tip and Ring to other signals = 100 mils
4. Route Tip and Ring on one layer only (top or bottom)
5. Module internal cables wire size = 26 AWG (stranded or twisted pair wire)

waiting to check

change name for ED5

copy ED5 to FX2

Waiting to check

delete Bluetooth
for defeature
EC & FALSH ROM

HWPG 591 => NB_PWRGD => EC_PWRGD
NORTH BRIDGE SOUTH BRIDGE
8Mbit (1M Byte), SPI

Each channel is 1A

Place ESD diodes as close as USB connector.

Reserve 0.1uF cap on USB_OC4-6# per EMC.

add for EMI suggestion:
0502 - swap P0/P2 traces as "fx2-swap-0502"

Waiting to check

change name for ED5
copy ED5 to FX2

Waiting to check
0427 : add 3 pads for EMI need

0505 : delete PV12 , caused interference with power component . EMI confirm no concern

0502 : reserve 20 pcs of 4700pF stiching Cap. from +1.8V_SUS to GND for EMI concern

place close to CPU

place close to DDR II connector

change footprint from "TH16H-C110D110N" to "TH16H-C197D63P2-8".
change name for ED5
copy ED5 to FX2
Waiting to check

Touch Pad

PMI media board changed to TP only as TPS
check EC for GPIO connection.
Refer to M07_LOM4401_X06 schematic.

Close to power pins
0.10*13 pcs

Place C607 close to pin65
Refer to M07_LOM4401_X06 schematic.

EMI requirement on 0812

Waiting to check

These three pin
LINK_LED100$, LINK_LED100$, ACT_LED are
open-drain type.

change name for ED5

copy ED5 to FX2

Note: BCM4401 requires
16-bit R/W data width.

Note: The BCM4401 has weak internal pull-down resistors on
the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
change name for ED5  
copy ED5 to FX2  
Waiting to check  
copy DM5 to FX2  

Copy _0407 Single Net, need to connect to 97551 port. Wait for BIOS team define.

Populate R492 0 ohm to disable WOL support at S5, enable WOL support at S3
**TABLE 1**

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<th>ADAPTER (W)</th>
<th>TRIP CURRENT (A)</th>
<th>PR20</th>
<th>PR25</th>
<th>PR26</th>
<th><strong>PR23</strong></th>
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<tr>
<td>65</td>
<td>3.17</td>
<td>57.6K</td>
<td>13K</td>
<td>105</td>
<td>N/A</td>
</tr>
<tr>
<td>90</td>
<td>4.43</td>
<td>51.1K</td>
<td>17.6K</td>
<td>348</td>
<td>33.2K</td>
</tr>
<tr>
<td>130</td>
<td>6.43</td>
<td>32.4K</td>
<td>20.5K</td>
<td>100</td>
<td>27.4K</td>
</tr>
<tr>
<td>150</td>
<td>7.43</td>
<td>30.9K</td>
<td>24.9K</td>
<td>432</td>
<td>88.7K</td>
</tr>
</tbody>
</table>

**PR23 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.**

For GPRS immunity place as close to the IC as possible.
Power On Sequence

- +3.3V_SUS
- +3V_SSRC
- SS_ON
- +3V_SS
- +1.2V_SS
- POWER SW# >200ms
- POWER)#
- SUSON,SUSD
- +3.3V_SUS
- +1.8V_SUS
- +0.9V_DDR_VTT
- +5V_RUN
- +3.3V_RUN
- +1.8V_RUN(CPU_PWR)
- +1.2V_VCCP(NB core)
- NB_PWRGD
- NB_PWRGD (SB_PWRGD)
- +VCC_CORE
- VDGT_RUN_ON
- +1.2V_VCCP(NB core)
- NB_PWRGD
- EC_PWRGD (SB_PWRGD)
- CPU_PWRGD
- PCB# (SB_RST#)
- ALINK_RSTW
- PCIRST#
- LDT_RST#
- LDT_STOP#

T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD
T9: SB_PWRGD to PCIRST#
T9C: PCIRST# to LDT_RST#
AC Only Power On Diagram

(1) +3.3V_SRC → (8) SUSON, SUSD
(2) SS_ON → (9) +5V_SUS
(3) +3V_SS, +1.2V_SS → +0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(4) RSMRST → (10) MAINON
(5) POWER_SW# → (11) +5V_RUN, +3.3V_RUN
(6) DNBSTON# → +2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(7) SUSC, SUSB# → (12) VRON
(13) +VCC_CORE → (14) CPU_COREPG
(15) VLDRT_RUN_ON → (16) +1.2V_VCCP
(17) HWPG_1.2V → (18) NB_PWRGD
(19) NB_PWRGD
(20) CPU_PWRGD
(21) PCI_RST# → (22) LDT_RST# → (23) LDT_RST#