PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.

VLDT_RUN

LAYOUT: Place bypass cap on topside of board near HT power pins that are not connected directly to downstream HT device, but connected internally to other HT power pins. Place close to VLDT0 power pins.
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE
10/15 Change the PN by Bevis

Change USBON# from 24 pin to 20 pin

USBON#<11> +3VPCU

2/20/08' Change PN from DFHD20MS025 and footprint

Change USBON# from 24 pin to 20 pin

USBON#<11> +3VPCU

Input sense resistor and Constant power setting table

<table>
<thead>
<tr>
<th>Power</th>
<th>65W</th>
<th>90W</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>20Ω Ohm CS020AGMD0</td>
<td>20Ω Ohm CS020AGMD0</td>
</tr>
<tr>
<td>R2</td>
<td>11.5K Ohm CS37153QF17</td>
<td>6.19K Ohm CS261993F23</td>
</tr>
<tr>
<td>R3</td>
<td>10K Ohm CS31003F949</td>
<td>10K Ohm CS31003F949</td>
</tr>
</tbody>
</table>

CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A

CURRNT LIMIT POINT = (65w/19v) * 0.85 = 2.907A
The image contains a schematic diagram of an electronic circuit. The diagram includes various components such as resistors, capacitors, diodes, and transistors, arranged in a network. The components are labeled with their values and configuration. The schematic is likely related to a specific electronic system or device, with annotations indicating connections and functionality. The text on the diagram includes symbols and descriptions that are standard in circuit diagrams, used to represent electrical connections and properties. The diagram does not appear to include any natural language text beyond the labels and symbols used for the circuit components.
VOUT=(1+R1/R2)*0.75

Rds*OCP=RILIM*20uA

Ton=3.85p*Ron+Vout/(Vin-0.5)

Frequency=Vout/(Vin*Ton)

Fds6690as Rds=12~15mOhm

OCP=7A

Frequency=(Vout/(Vin*Ton))

Plastic=12m*6=RILIM*20uA

RILIM=3.6K(2.5~8K)
VOUT = (1 + R1/R2) * 0.75  

\[ R_{ds} \times OCP = R_{ILIM} \times 20 \mu A \]

\[ V_{OUT} = 1.5V \]

\[ F_{DS6690AS} \ R_{ds} = 12 \sim 15 \Omega \]

\[ OCP = 7 \sim 0.8 \ A \]

\[ T_{ON} = 3.85p \times R_{TON} \times V_{out} / (V_{in} - 0.5) \]

\[ F_{requency} = V_{out} / (V_{in} \times T_{ON}) \]

\[ T_{ON} = 3.85p \times 1M / (V_{in} - 0.5) \]

\[ F_{requency} = 1 / (0.0036767) = 272K \]

\[ I_{(ripple \ current)} = (19 - 1) / (2.2u \times 272K \times 19) = 1.58A \]

\[ 12m \times 6 = R_{ILIM} \times 20 \mu A \]

\[ R_{ILIM} = 3.6K (2.5 \sim 8K) \]
Vout=0.75/(1+R1/R2)
if tune Vout PR38
un-mount, PR156
PR165 mount

8/27 Add CAP for Delay time.

FDS6690AS Rds=3.8~4.6mOhm
OCP=12~0.5A
I_{rippled current} = (19-1.8)*1.8/(2.2u*400k*19)
~1.03A
3.8m*12=RILIM*10uA
RILIM=4.56K
(10u*PR35/Rdson+Delta_I/2=Iocp

OCP: 12.5A

FDS6690AS Rds=3.8~4.6mOhm
OCP=12-0.5A
I\_rippled current = (19-1.8)*1.8/(2.2u*400k*19)
\sim 1.03A
3.8m\times12=\text{RILIM}\times10uA
\text{RILIM}=4.56K
(10u\times PR35)/\text{Rdson}+\Delta I/2=I_{ocp}
1. +1.1V_SSMCP77M Power (+1.1V_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER (S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V_SSMCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C, SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBttooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCFP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5V CPU VDDA
9. +3V_LANLAN Power (BCM5764M)
10. +1.2V_LANLAN Power (BCM5764M)
11. +2.5V_LANLAN Power (BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VUSUSCPU VDD I/O, System Memory
14. SDMDDR_VTEMCPU Memory Interface, SYSTEM DDR DIMM Memory Termination
15. +1.8V MCP77M LCD Interface
16. +1.1V_NBMCPP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB_COREMCP77M Core Power
18. +1.2V_HTCPU HT Power
19. CPU_CORE0 CPU Power
20. CPU_CORE1 CPU Power
21. CPU_VDDNB_RUNCPU NB Power
22.