2.5A

S/N doesn't define it yet.
Vcc Core Decoupling Caps
Place these on bottom side.

For EMI requirement.
Place the CAPs on the nook of Vcore and other power planes.

VSSSENSE and VCCSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

Place pull-up/down resistors within 1 inch of CPU.
Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fanspeed accuracy.

Place U401 near CON401

Open-drain

------------------OTHER SIGNALS

12 mils===============GND    10 mils=========H_THERMDA(10 mils)    10 mils=========H_THERMDC(10 mils)    10 mils=========GND    12 mils---------------------OTHER SIGNALS

Avoid BPSB, Power

Route H_THERMDA and H_THERMDC on the same layer

SMBus Address: 5Ch

Monitors processor core voltage (0 – 3V)

Pin 10 & Pin 24 set inverting PWM Mode

Set INV=1 to invert PWM output

Route H_THERMDA and H_THERMDC on the same layer

OTHER SIGNALS

12 mils

GND

10 mils

H_THERMA(10 mils)

10 mils

H_THERMDC(10 mils)

10 mils

GND

12 mils

OTHER SIGNALS

Avoid BPSB, Power

Title: THER-SENSOR.FAN

Engineer: Marco Chen

ASUSTeK COMPUTER INC
When using Intel® 955X, 945PM/GM and 940GML Express Chipset platform with external graphics only, IREF resistor is not required.
CFG5 : DMI STRAP
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG11 : PSB 4X CLK ENABLE
LOW = REVERSAL
HIGH = Calistoga (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION

CFG10 : HOST PLL VCO SELECT
LOW = RESERVED
HIGH = MOBILITY

CFG15 : ICH RESET DISABLE
LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION

CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Enabled (Default)

CFG18 : GMCH Core Voltage Level
LOW = 1.05V (Default)
HIGH = 1.5V

CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[20..18] have internal pulldown resistors.
SDVOCRtl_DATA has internal pulldown resistors.
INVERTER interface

**BIOS BACK_OFF#:** When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.

**BIOS INV_DA:** KBC output D/A signal (adjust voltage level) to adjust Back light.

A6J uses D1 R:1.0 Inverter Board

A6J doesn't support USB WLAN function!
Address reference +1.8V, add four 0.1uF decoupling CAP.

SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1.
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS
(Linein) FL = 7.2 Hz
(Linein) FH = 174.98K Hz

(Lineout) FL = 7.2 Hz
(Lineout) FH = 174.98K Hz

Fix POP of the internal speaker
when power-off

Fix POP of the internal speaker
when power-on

Headphone & SPDIF JACK

Title: Audio AMP
Engineer: Marc Chen
PS5_44, PS5_43, PS5_40 are wakes up event inputs when KBC in standby mode.
LAN PORT

LAN SWAPED-1013

MDC

Must change to 13-N7510M270
1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5 mm
4. No via recommend, maximum is one
5. Total length < 50 mm
6. Differential impedance is 110 ± 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25 mm

1. Soft start
2. Place as close to card reader socket as possible

Layout: SHIELD GND

Soft start
Place as close to card reader socket as possible
### SM-Bus Address Table

<table>
<thead>
<tr>
<th>Host</th>
<th>SM-Bus Device</th>
<th>SM-Bus Address</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICH7-M</td>
<td>Clock Generator</td>
<td>11010001x (D2)</td>
<td>ICS954310</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>SO-DIMM 0</td>
<td>10100000x (A0)</td>
<td>DDR SOCKET1</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>SO-DIMM 1</td>
<td>10100001x (A4)</td>
<td>DDR SOCKET2</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>Thermal Sensor</td>
<td>01011100x (SC)</td>
<td>ADT7463 (Optional)</td>
</tr>
</tbody>
</table>

### PCI Device Table

<table>
<thead>
<tr>
<th>PCI Device</th>
<th>IDSEL#</th>
<th>REQ/GNT#</th>
<th>Interrupts</th>
</tr>
</thead>
<tbody>
<tr>
<td>CARDBUS</td>
<td>AD17</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>CARD READER</td>
<td>AD17</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>1394</td>
<td>AD17</td>
<td>1</td>
<td>D</td>
</tr>
</tbody>
</table>
R1.0 -> R1.1

1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#

2. Page4: Modify FAN solution from DA to PWM and change R-C delay timing.
   A. Mount R416 and DNI R415
   B. Change C404 to 1uF

3. Page4: Connect +3V5_FAN(R419*3.3K ohm and R420*2.2K ohm) from +V5S_FAN to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3V5 and U401.3 level shift from 5V to 3V

4. Page4: Add pull-down resistor R418*10M ohm to protect noise when power-on

5. Page4: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock

6. Page5: Add pull-down resistor R531 from 10 ohm to 22ohm to eliminate swing.


9. Page5: Change L905 to P/N:09G012030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.


11. Page6: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VB105 support.

12. Page6: Add R1343*0 ohm for reserving bead to ground.

13. Page15: Change L1504.2 to connect to +VGA_VCORE to +1.2VS for ATI recommendation.

14. Page15: Change bead L1506 from 1200hm/100mhz to 300hm/100mhz type.

15. Page19: Add bead L1913 between TV_GND and GND.

16. Page23: Change High Definition damping resisters*R2312, R2314, R2316, R2318, R2320, R2322, R2334, R2335 to 22 ohm or 39 ohm for reducing reflection.


18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.

19. Page34: Add Q3401 and R3414 to replace R1344, please comment Black 3.

20. Page41: Change S4 strech circuits, please comment Block 4.


23. Page42: Change CON4021.1 and CON4021.2 power from +3VUS to +3V.

24. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.

25. Page7: Change from VRM_PWROK to ICH7_PWROK to enable MCH_PWROK for Intel requirement(Mount R721 and DNI R722).

   A. Mount R2315 and DNI R4507
   B. Remove the circuits.(please comment Block 5)
   C. Mount thermal protection circuits.(please comment Block 6)

33. Page5, 23, 37: Change capacitor values for TXC recommendations(C513, C514 from 33pF to 27pF, C3202, C3204 from 12pF to 22pF ,Change X3701 to 07G010S22450*30 ppm and C3725 and C3726 to 22pF).

34. Page5, 47: Add Back Bias circuits for ATI recommendations.


37. Page39: Reserve R-C to tune waveform question.(R3906,R3907,C3911,C3912)

38. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.

R1.1 -> R2.0

1. Page4, 34: Add power limit solution and change thermal protection solution.
   A. Add R421*0 ohm and connect to H_PROCHOT_S#
   B. DNI R417*0 ohm
   C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.
   D. DNI DNI 013120120409.


3. Page15: Short R2704 from 0 ohm to 150 ohm.


6. Page30: Add KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.

7. Page36: Change CARDBUS chip reset signal from PLT_RST#_BUF to PLT_RST#. (Mount R3618 and DNI R3617).

8. Page39: Change WLAN_LED# pull-high resistor R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

   A. Mount R2315 and DNI R4507
   B. Remove the circuits.(please comment Block 5)
   C. Mount thermal protection circuits.(please comment Block 6)


12. Page9: Reserve R-C to tune waveform question.(R3906,R3907,C3911,C3912)


14. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.
15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.
16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

**VGA NV G72M-V** R1.0 -> R1.1

1. Page15: Change R1507 from 121 ohm to 0 ohm and Remove R1511 for SSC 3.3V requirement.
2. Page13: Change VRAM CLK Terminators R1303, R1304 from 120 ohm to 100 ohm for NV recommendation.
3. Page14: Change VRAM CLK Terminators R1402, R1403 from 120 ohm to 100 ohm for NV recommendation.
5. Page17: Mount SGIO_PADCFG R1720 and DNI R1721 for NV recommendation.
6. Page17: Change RN1701 from 470 ohm to 470 ohm for BOM issue.
7. Page19: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
8. Page43: DJ_LED# Pull high to +3V via R4327 10Kohm.
11. Page34: Change C3404 RN5VD to CMOS Topology and R3402(DNI).
12. Page34: Change R420 from 22K ohm to 10K ohm and change R419 from 33K ohm to 20K ohm for Volt divide.
13. Page43: Mount R4301
15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.
16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

**VGA NV G72M-V** R1.0 -> R1.1

1. Page15: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
2. Page31: Change C3133,C3134 from 22PF to 27PF.
3. Page25: Add R2550 ,R 2553, R2555 for BT_ON.
5. Page17: Change RN1701 from 4R8P 0603 to 4R8P 0402 for BOM issue
6. Page17: Add U3003, Q3008(DNI) for 4S1P Battery detected.
7. Page19: Change L1901, L1905, L1906 to 180NH.
8. Page19: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
11. Page34: Change C3404 RN5VD to CMOS Topology and R3402(DNI).
12. Page34: Change R420 from 22K ohm to 10K ohm and change R419 from 33K ohm to 20K ohm for Volt divide.
13. Page43: Mount R4301
15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.
16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

**VGA NV G72M-V** R1.0 -> R1.1

1. Page15: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
2. Page31: Change C3133,C3134 from 22PF to 27PF.
4. Page45: Change C4509 from 10uf to 2.2uf.
5. Page19: Change R1910 from 33Kohm to 47Kohm for BOM reduction.
6. Page15: Change R1501 from 71.5ohm to 81.6ohm for BOM reduction.
7. Page25: Add R2550 ,R 2553, R2555 for BT.ON.
For foldback current limit

VILIM = 0.43V, OCP = 18A

VFB = 0.7V

Ipp = 3.572A

R2.2

Custom

Title: POWER_I/O_DDR & VTT

Engineer: Charise/Mia

A6JC
Model | VGA | +VGA_CORE | R5506 | R5507 | R5510
--- | --- | --- | --- | --- | ---
A6JC | G72M-V | 1.0V | 0 | 100K | @
A6JM | G73M | 1.1V | 10K | 100K | @
TOTAL POWER=65W

200mAh  41.2K   1.8976   1.39
220mAh  52.3K   2.0889   1.537
240mAh  66.5K   2.2918   1.679
260mAh  86.6K   2.4871   1.822

Adaptar error circuit for 4S battery

Power Limit Circuit

Pre-charge voltage 12.6V