Alviso Strapping Signals and Configuration

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Strap Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFG[2:0]</td>
<td>FSB Frequency Select</td>
<td>000 = Reserved, 001 = FSB53, 010 = FSB800, 011 = Reversed</td>
</tr>
<tr>
<td>CFG[1:0]</td>
<td>Reversed</td>
<td></td>
</tr>
<tr>
<td>CFG3</td>
<td>DDR III Select</td>
<td>0 = DDR II, 1 = DDR I</td>
</tr>
<tr>
<td>CFG4</td>
<td>DDR I / DDR II</td>
<td>1 = DDR I</td>
</tr>
<tr>
<td>CFG7</td>
<td>CPU Strap</td>
<td>1 = Desktop</td>
</tr>
<tr>
<td>CFG[12:11]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG[14:13]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG[16:15]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG[17]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG[18]</td>
<td>CPU core Vol Select</td>
<td>0 = 1.05V</td>
</tr>
<tr>
<td>CFG[19]</td>
<td>CPU Vtt Select</td>
<td>1 = 1.8V</td>
</tr>
<tr>
<td>CFG20</td>
<td>SDVO Present</td>
<td>0 = No SDVO device present</td>
</tr>
</tbody>
</table>

ICH6-M Integrated Pull-up and Pull-down Resistors

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Strap Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACE_BIST_CLK</td>
<td>DPPSLP#, EE_DIN</td>
<td>ICH6 internal 20K pull-ups</td>
</tr>
<tr>
<td>EE_DOUT, GNT[5:0]/GPO[17], GPP[6]/GPO[16], LBDR[1]/GPI[41], LAD[3:0]/FR[3:0], LDRQ[0], TWE#, PME#/#TF[3]</td>
<td>ICH6 internal 10K pull-ups</td>
<td></td>
</tr>
<tr>
<td>LAN_RDX[2:0]</td>
<td>ICH6 internal 20K pull-downs</td>
<td></td>
</tr>
<tr>
<td>ACE_EDT#</td>
<td>ACE_BIST#2:0, ACE_SYNC</td>
<td>ICH6 internal 20K pull-downs</td>
</tr>
<tr>
<td>SPP#, EX_CS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB[7:0][#P,#N]</td>
<td>ICH6 internal 11.5K pull-downs</td>
<td></td>
</tr>
<tr>
<td>DDP[7:0][#P,#N]</td>
<td>(Default)</td>
<td></td>
</tr>
<tr>
<td>LAN_CLK</td>
<td>ICH6 internal 100K pull-downs</td>
<td></td>
</tr>
</tbody>
</table>

ICH6-M IDE Integrated Series Termination Resistors

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Strap Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>D3[15:0], DIO#, DIO#, DREQ, DCAM#, DORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ</td>
<td>approximately 33 ohm</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK in signal.
Layout Notes:

- VCCSENSE and VSSSENSE lines should be of equal length.
- Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9 ohm resistors terminate the 55 ohm transmission line.
Place Test PAD Near to Chip as could as possible

Place Test PAD Near to Chip as could as possible
Place these Hi-Freq decoupling caps near GMCH
Put decap near power (0.9V) and pull-up resistor

Decoupling Capacitor

Place these Caps near DM1

Place these Caps near DM2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
**CRT CONNECTOR**

Ferrite bead impedance: 75ohm@100MHz

50 Ohm Impedance 75 Ohm Impedance

Hyxnc & Vsync level shift

DDC_CLK & DATA level shift

ESD Protection Diode

<Core Design>

Wistron Corporation

3F, 36, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Date: February 15, 2006

Sheet 4 of 6

Title: CRT Connector

Size Document Number Rev

Custom

Date: Sheet

Date: Sheet

Date: Sheet

MYALL SA
**USB PORT**

**MYALL SB CHANGE TO 100U+2 FROM 150U.**

**BLUETOOTH MODULE**

**MDC 1.5 CONNECTOR**

**Change To AZ**

1st source: 20.D0197.144

2nd source: 20.F0604.012

MYALL DIS 0206

USB / MDC / BLUETOOTH

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias. No 90 degree bends.
4. Pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

LAN Connector

3D3V_85 add 0.1u near LAN1 by EMI request
NEED PUT SOCKET
P/N AND FLASH
ROM P/N IN BOM

72.39040.H03 FOR LEAD FREE
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
U2762.10054.051SOCKET

Board ID

Keyboard matrix (from vendor)

Low Bit

High Bit

<table>
<thead>
<tr>
<th>US</th>
<th>Jap</th>
<th>Kur</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
1. U12, U14: AO4422 84.04422.037
   U13, U15: AO4430 84.04430.037
   R100: 3K8R3F-GP

2. U12, U14: IRF7413 84.07413.037
   U13, U15: IRF7832-U 84.07832.037
   R100: 2K43R2F

12.4uA/0.87/0.5 = 28.54uA
Rds(on) * Io = Isen * Resen
(5m/2) * 25A = 28.54uA*Resen
R33 = 2.18K ~ 2.15K

Load Line Slope: 3mR
515mV/1uA = 75mV
Idrop = 75mV / 6.04K = 12.4uA

Wistron Corporation
Taipei Hsien 221, Taiwan, R.O.C.

Title: MYALL
Size: A3
Document Number: 34
Rev: 0
Date: Thursday, February 10, 2006
Sheet: 34
Ioc = 40uA*Roc/Rds

Roc close high side MOS Drain pin

Vout = 0.8V(1+Rout/Rgnd)

0D9V

1 MYALL DIS 0206

16.29 PM, SUP, SAG

16,18,24,32,38,41,42 PM, SUP, SAG

DDR_VREF, S3

VDD, VISION, S3

GND, S3

1 MYALL DIS 0206

16.29 PM, SUP, SAG

16,18,24,32,38,41,42 PM, SUP, SAG

DDR_VREF, S3

VDD, VISION, S3

GND, S3
Page 40 of the EMI of capacitor and spring, can delete first by EMI request.
The R784 (XTALSSN 106) pull-down) should be NO STUFF when spread chips is used.
Dummy R784

50 ohm trace to filter
37.5 ohm trace to 150R resistor
CLOSE TO G72

PLACE R318 CLOSE TO G72 MYALL SB
MYALL SB CHANGE

2004/11/10 CHANGE TO 3D3V_S0

2004/11/10 ADD 220 Ohm at 100MHz
"Place the differential termination resistor at the end of the transmission line."

Decoupling for left MEMORY
Place around the MEM

Decoupling for right MEMORY
Place around the MEM

---

Title:
Size:
Doc.
Rev.

Date: Friday, February 10, 2006

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Core Design
Decoupling for left MEMORY
Place around the MEM

Decoupling for right MEMORY
Place around the MEM

* "Place the differential termination resistor at the end of the transmission line*
For MEM strapping, please use below table,

<table>
<thead>
<tr>
<th>RAM_CPU[3:0]</th>
<th>Config</th>
<th>FB Bus Width</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td></td>
<td>64-bit</td>
<td>Elpida</td>
</tr>
<tr>
<td>0001</td>
<td>16Mx64 DDR2</td>
<td>64-bit</td>
<td>Samsung</td>
</tr>
<tr>
<td>0010</td>
<td>16Mx64 DDR2</td>
<td>64-bit</td>
<td>Infineon</td>
</tr>
<tr>
<td>0011</td>
<td>16Mx64 DDR2</td>
<td>64-bit</td>
<td>Hynix</td>
</tr>
</tbody>
</table>
Vref = 0.6V
Vo = (1+R8/R9)*0.6V =1.5V