Layout Note:

- Coupo, 2 connect with IO=274 ohm, make trace length shorter than 0.5".
- Coupo, 3 connect with 20=54.9 ohm, make trace length shorter than 0.5".

PROCHOT# is not supported.

S/W doesn't define it yet.
**VCC Core Decoupling Caps**

Place these on bottom side.

For EMI requirement.
Place the CAPs on the topside only.

- **VCCSENSE** and **VSSSENSE** trace at 27.4 ohm with 25 mils spacing mismatch and 18 mils trace on 7 mils spacing.
- Place pull-up/down resistors within 1 inch of CPU.

**VCCSENSE** and **VSSSENSE** trace at 27.4 ohm with 25 mils spacing mismatch and 18 mils trace on 7 mils spacing.

- Place pull-up/down resistors within 1 inch of CPU.
Fan Speed Control

Using an OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

Place U401 near CON401

CPU Fan

Monitor processor core voltage (0 – 3V)

Open-drain

Pin 10 & Pin 24 set inverting PWM Mode
Set INV=1 to invert PWM output

Adapted from ADT_D2-FAN_PWM# and ADT_D2+

NDT 20.64 SMBus Address: 5Ch

Open-drain

Avoid BPSB, Power

Route H_THERMDA and H_THERMDC on the same layer

OTHER SIGNALS

OTHER SIGNALS

OTHER SIGNALS
When using Intel® 955XM, 945XM/QM and 945GML Express Chipset platform with external graphics only, IREF resistor is not required.
CFG5 : DMI STRAP
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG11 : PSB 4X CLK ENABLE
LOW = REVERSAL
HIGH = Calistoga (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION

CFG10 : HOST PLL VCO SELECT
LOW = RESERVED
HIGH = MOBILITY

CFG15 : ICH RESET DISABLE
LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION

CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : GMCH Core Voltage Level
LOW = 1.05V (Default)
HIGH = 1.5V

CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[20..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.
Cable Requirement:
- Impedance: 100 ohm +/- 10%
- Length Mismatch <= 10 mils
- Twisted Pair (Not Ribbon)
- Maximum Length <= 16"
Address reference +1.8V, add four 0.1uF decoupling CAP.

SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1.
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS
<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe xx</td>
<td>PCI stretching</td>
<td>Provides additional PCIe lanes</td>
</tr>
<tr>
<td>*VCC</td>
<td>VCC power</td>
<td>Supplies power to the circuitry</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>Connects to the ground</td>
</tr>
</tbody>
</table>

**Diagrams:**
- Place near PCI Bus:
  - Components labeled with their respective functions such as PCI, REQ, GNT, C/BE, IRDY, etc.
- Interrupt I/F:
  - Details on interrupt signals like PCI_INTA, PCI_INTB, etc.
- Miscellaneous:
  - Additional components and connections relevant to the PCI system.
(Linein) FL = 33.9 Hz
(Linein) FH = 23.4K Hz

(Headphone Mode) FL = 15.9Hz
(Headphone Mode) FH = 23.4K Hz

Fix POP of the internal speaker when power-off
Fix POP of the internal speaker when power-on

Headphone & SPDIF JACK

Audio AMP

*Variant Name*
Internal MIC Pre-Amplifier

(Microphone) FL = 33.86 Hz
(Microphone) FH = 27.2K Hz
PS4, PSS, P43, P50 are wake-up event inputs when KBC in standby mode
1. Close to R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5 mm
4. No via recommended, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110 +/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25 mm

Place as close to card reader socket as possible.
Pin width=23mils
4P2R array resister
cou- layout with common choke
PLCC32 Socket Part Number: 12-043000323
SST FWHLPC Part Number: 05G00101712L(12)

Startup Circuit 2.0

Title: Startup Circuit

Engineer: Marco Chen

Sheet A6J

Date: November 24, 2005

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<table>
<thead>
<tr>
<th>Host</th>
<th>SM-Bus Device</th>
<th>SM-Bus Address</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICH7-M</td>
<td>Clock Generator</td>
<td>1101001x (D2)</td>
<td>ICS954310</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>SO-DIMM 0</td>
<td>1010000x (A0)</td>
<td>DDR SOCKET1</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>SO-DIMM 1</td>
<td>1010001x (A4)</td>
<td>DDR SOCKET2</td>
</tr>
<tr>
<td>ICH7-M</td>
<td>Thermal Sensor</td>
<td>0101110x (5C)</td>
<td>ADT7463 (Optional)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PCI Device</th>
<th>IDSEL#</th>
<th>REQ/GNT#</th>
<th>Interrupts</th>
</tr>
</thead>
<tbody>
<tr>
<td>CARD READER</td>
<td>AD17</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>CARDBUS</td>
<td>AD17</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>1394</td>
<td>AD17</td>
<td>1</td>
<td>D</td>
</tr>
</tbody>
</table>
R1.0 -> R1.1
1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#

2. Page4: Modify FAN solution from DA to PWM and change R-C delay timing.
   A. Mount R416 and DNI R415
   B. Change C404 to 1uF
3. Page4: Connect +3VS_FAN(R419*3.3k ohm and R420*2.2k ohm from +VSS_FAN) to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3VS and U401.3 level shift from 5V to 3V
4. Page4: Add pull-down resister R418*10M ohm to protect noise when power-on
5. Page5: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock
6. Page5: Change R531 from 10 ohm to 22ohm to eliminate swing.
9. Page9: Change L905 to P/N:09G0112030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.
11. Page13: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VBIOS support.
12. Page13: Add R1343*0 ohm for reserving bead to ground.
13. Page15: Change L1504.2 to connect from +VGA_VCORE to +1.2VSP for ATI recommendation.
14. Page15: Change lead L1506 from 120ohm/100MHz to 300ohm/100MHz type.
15. Page19: Add lead L1913 between TV_GND and GND.
18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.
19. Page34: Add Q4301 and R4314 to replace U3402B.
20. Page34,35: Modify reset circuits to meet Intel specification, please commit Black 3.
21. Page35,43 : DNI R4312 and change R3509 from 4.7M ohm to 2.2 M ohm to short SWDJ EN# detected to 2seconds for BIOS requirement and add INIT# solution (please comment Block 7).
22. Page37: Change R3706 from 10K ohm to 100K ohm to enlarge R-C delay time.
23. Page39: Reserve R3905 to PLT_RSTNS# Wire-Or with PLT_RST#_BUF.
24. Page41: Short CON4101.1 and CON4101.2 and delete R4105, R4104, and C4103 because no timing issue between power and enable signal.
25. Page42: Delete D4201 and DNI R4202 because no power loss issue exist.
27. Page44: Add TPM connector.
29. Page42: Change CON4202.1 and CON4202.2 power from +3VUS to +3V.
30. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.
31. Page7: Change from VRRM_PWRGD to 1CH7_PWROK to enable MCH_PWROK for Intel requirement (Mount R721 and DNI R722).

R1.1 -> R2.0
1. Page4, 34: Add power limit solution and change thermal protection solution.
   A. Add R421*0 ohm and connect to H_PROCHOT_S#
   B. DNI R417*0 ohm
   C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.
   D. DNI OTP solution.
2. Page15: Add BBIAS_CNTL pull-down resister R1508*10K ohm to GND.
4. Page24: Add 3 pcs decoupling CAPs(C2410, C2411, C2412) to short return path because PCI Bus(1N1) reference +1.8VS(Vcc).
5. Page25, 44: Add BT_LED solution to co-layout with Scroll Lock for Epson requirement.
6. Page27: Change R2704 from 0 ohm to 150 ohm.
7. Page27: Change R2707 from 47K ohm to 332K ohm.
   A. Change BAT_SEL# push-pull resister from +3V to GND.
   B. DNI Q3002*2N7002.
10. Page31: Change LAN chip reset signal from PLT_RST#_BUF to PLT_RST#_. (Mount R3107 and DNI R3106).
11. Page35: Change KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.
13. Page39: Add WLAN_LED# pull-high resister R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

15. Page 43: Mount R4301*100K ohm to avoid PWR_SW# is floating.

16. Page 43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.
\[ F = 300\text{KHz} \]

\[ I_{pp} = 3.572\text{A} \]

Apply 1.5UH P/N VILIM = 1.465V, OCP = 6.967A For foldback current limit